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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Leonard Forbes et al.

Title: TRANSISTOR WITH VARIABLE ELECTRON AFFINITY GATE AND METHODS OF FABRICATION AND USE

Docket No.: 303.324US2
Filed: February 23, 1999
Examiner: Michael Trinh



Serial No.: 09/256,643
Due Date: October 5, 2000
Group Art Unit: 2822

Commissioner for Patents
Washington, D.C. 20231

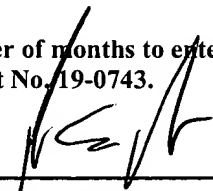
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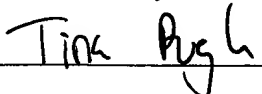
- X A return postcard.
- X An Amendment and Response (12 Pages).
- X A Supplemental Information Disclosure Statement (1 pgs.), Form 1449 (1 pgs.), and copies of 11 cited references.
- X A check in the amount of \$240.00 to cover the fee for consideration of Information Disclosure Statement under 97(c).

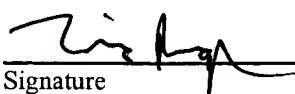
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on this 5 day of October, 2000.


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